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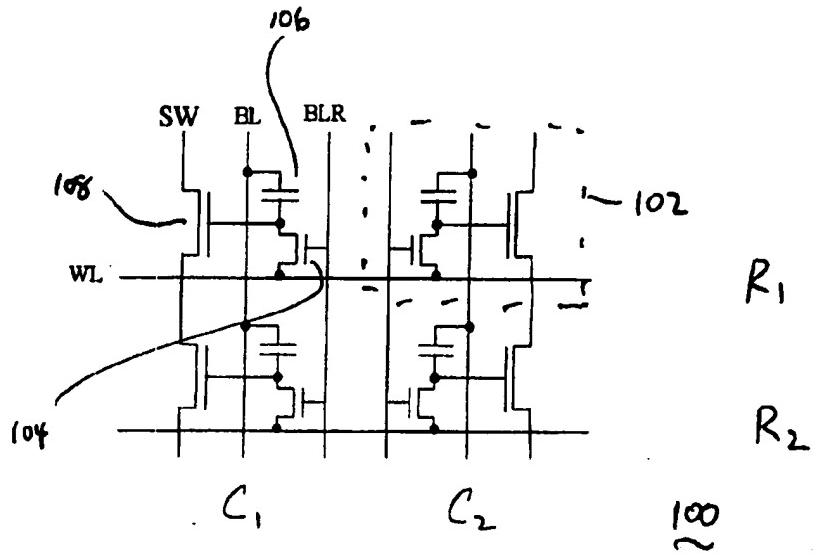


Fig. 1

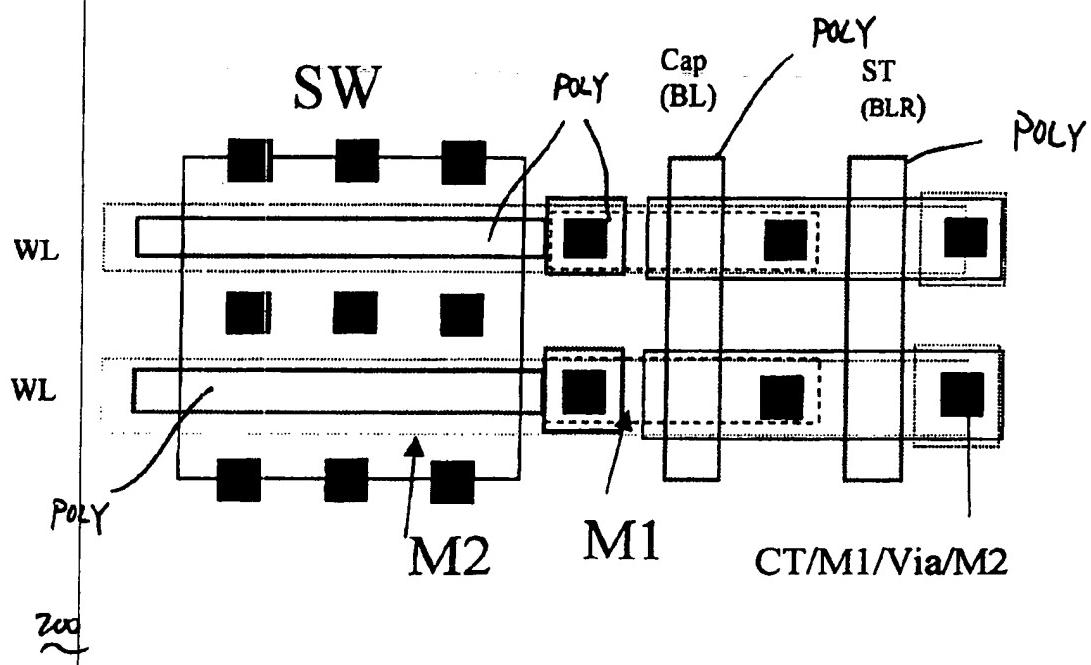


Fig 2

0.18um LV XPM FPGA Cell Operation						
		Vbl	Vblr	Vwl		Program
Program	SC/SR	8	3.3	0		Yes
	SC/UR	8	3.3	3.3		No
	UC/SR	0	0	0		No
	UC/UR	0	0	3.3		No
Read	SC/SR	1.8-3.3	1.8	0		Sense current
	SC/UR	1.8-3.3	1.8	1.8		Yes
	UC/SR	0	0	0		No
	UC/UR	0	0	1.8		No
Operation		1.8	0~0.8	0		

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Fig 3

0.18um IO XPM FPGA Cell Operation						
		Vbl	Vbr	Vwl		Program
Program	SC/SR	8	3.3	0		Yes
	SC/UR	8	3.3	3.3		No
	UC/SR	0	0	0		No
	UC/UR	0	0	3.3		No
Read	SC/SR	3.3	3.3	0		Sense current
	SC/UR	3.3	3.3	3.3		Yes
	UC/SR	0	0	0		No
	UC/UR	0	0	3.3		No
Operation		3.3	0.3-0.8	0		Yes

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Fig 4

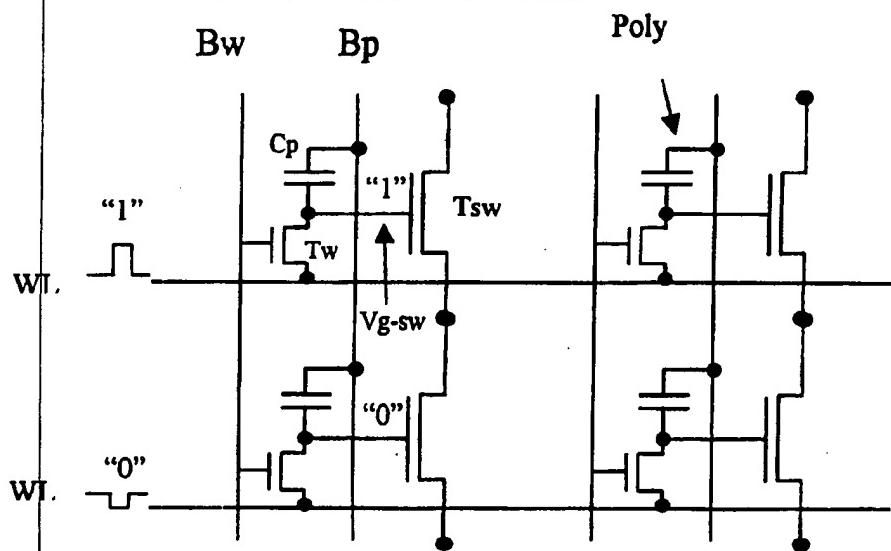


Fig 5

Dynamic XPM FPGA Cell Operation

		Vbw	Vbp	Vwl(1)	Vwl(0)
Write or Refreshing by columns	SC	Vcc	0	Vcc	0
	UC	0	0	Vcc	0

*SC- Selected Column; UC- unselected Column.

Fig 6

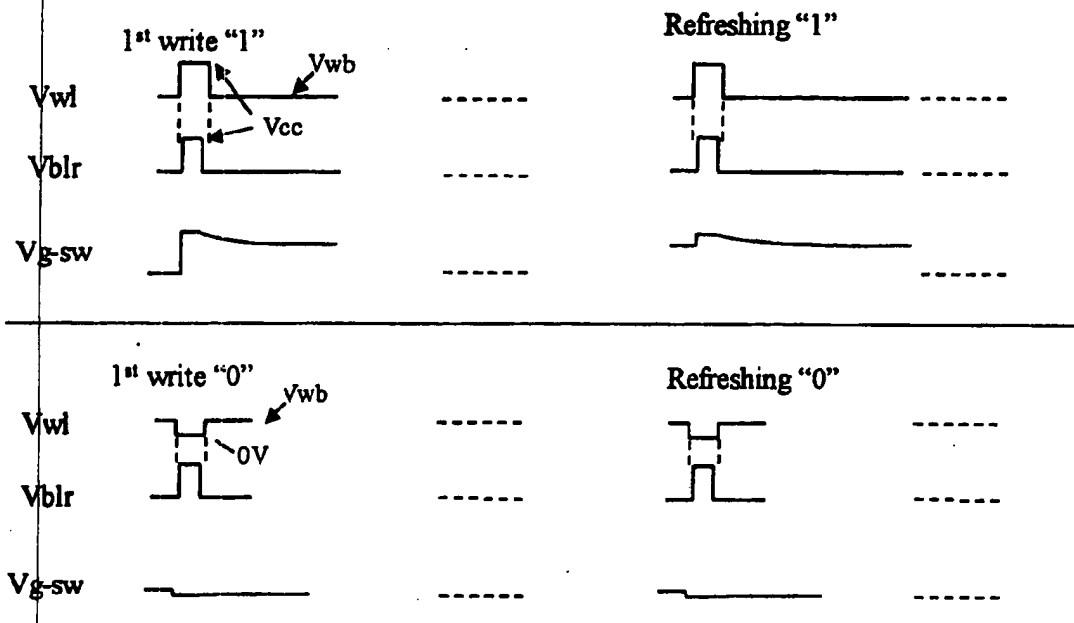


Fig 7

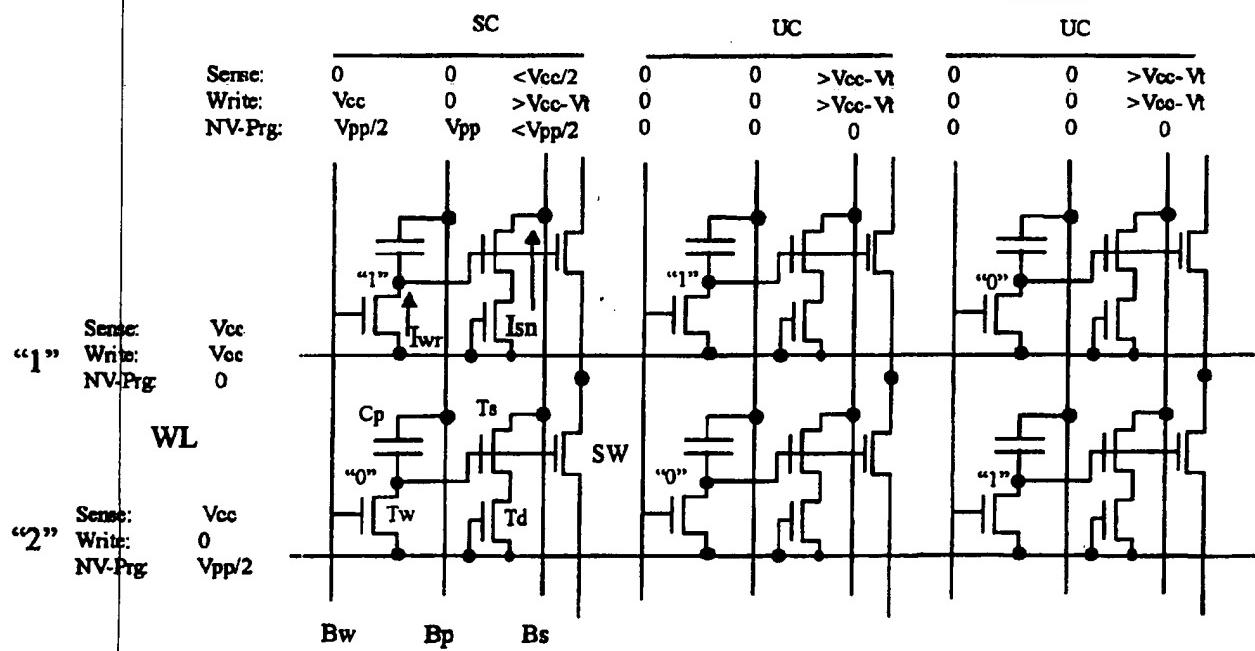


Fig 8

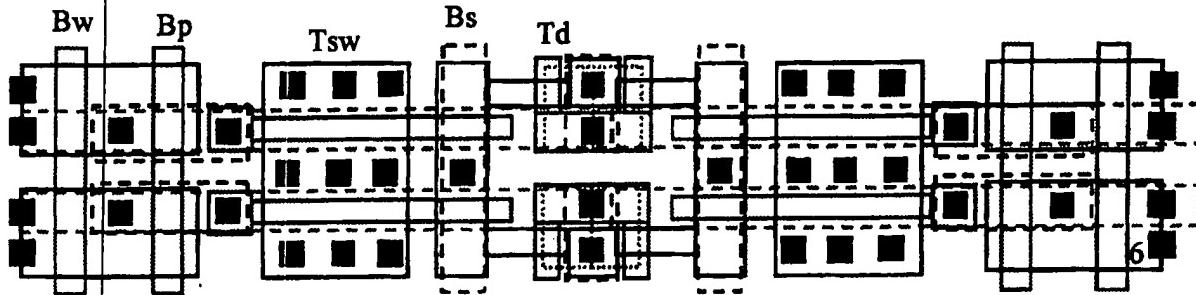


Fig 9

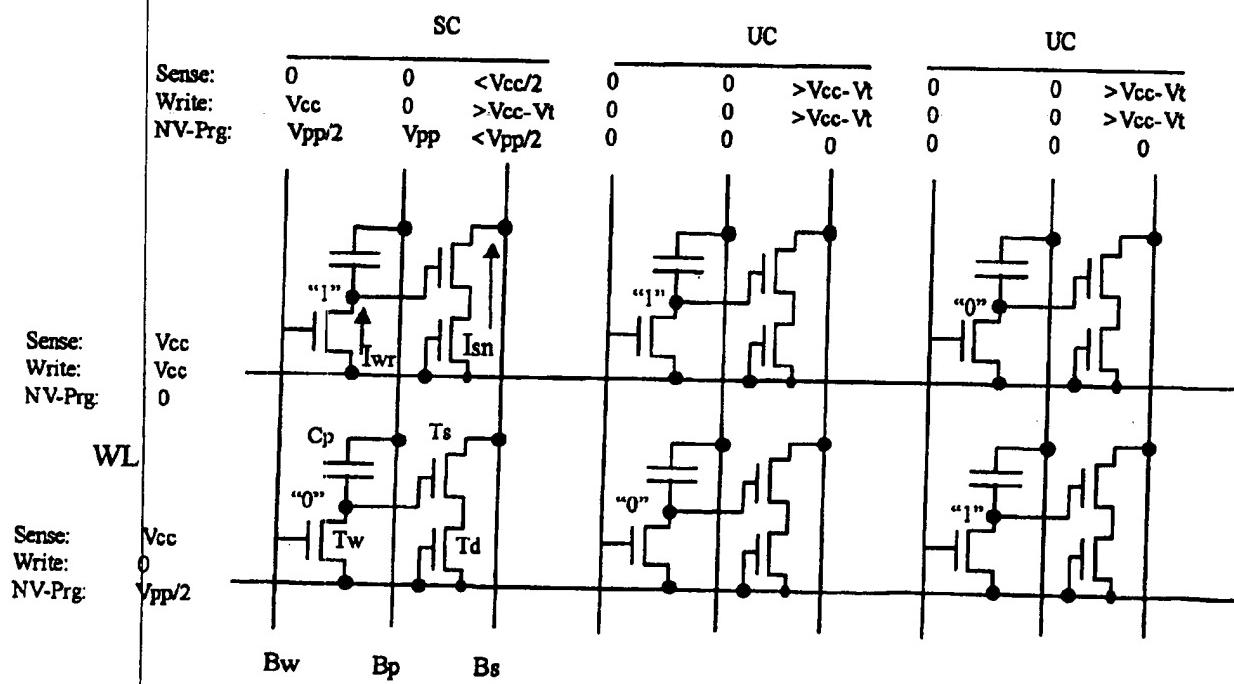


Fig 10

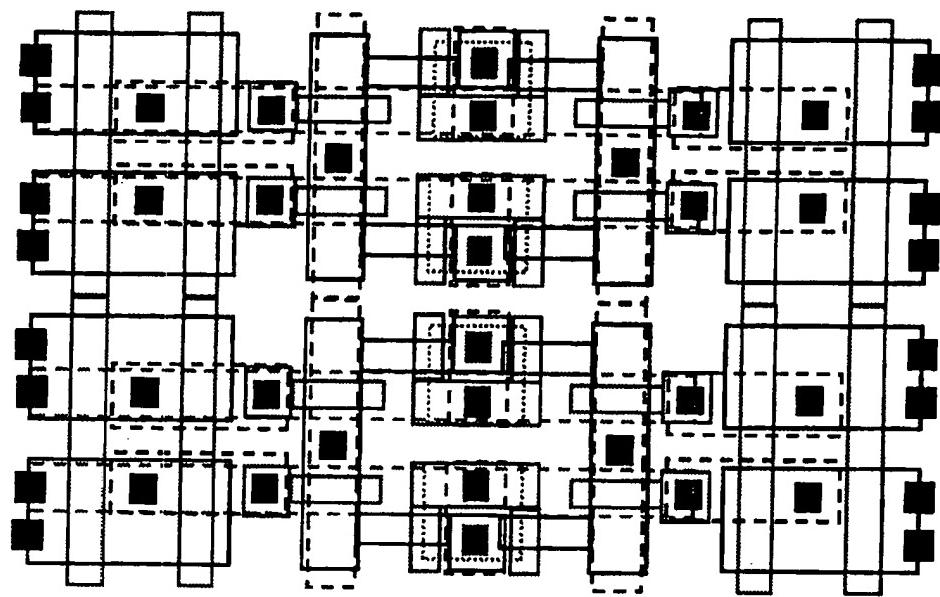


Fig 11